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FORM PTO-1449	SERIAL NO. 10/676,862	CASE NO. 10519-112
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (use several sheets if necessary)	FILING DATE September 30, 2003	GROUP ART UNIT
APPLICANT(S): So et al.		

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER <small>Number-Kind Code (if known)</small>	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
DL	A1	5,784,328	07/1998	Irrinki et al.		
	A2	5,149,199	09/1992	Kinoshita et al.		
	A3	5,977,746	11/1999	Hershberger et al.		
	A4	5,890,100	03/1999	Crayford		
	A5	US 2003/0046020 A1	03/2003	Scheuerlein		
	A6	6,525,953 B1	02/2003	Johnson		
	A7	6,185,121 B1	02/2001	O'Neill		
	A8	5,652,722	07/1997	Whitefield		
	A9	6,246,610 B1	06/2001	Han et al.		
	A10	US/2002/0136045 A1	09/2002	Scheuerlein		
	A11	US/2002/0136047 A1	09/2002	Scheuerlein		
	A12	5,835,396	11/1998	Zhang		
	A13	6,034,882	03/2000	Johnson et al.		
	A14	6,420,215 B1	07/2002	Knall et al.		
	A15	5,923,588	07/1999	Iwahashi		
	A16	6,407,953 B1	06/2002	Cleeves		
	A17	5,818,748	10/1998	Bertin et al.		
	A18	6,157,244	12/2000	Lee et al.		
	A19	4,646,266	02/1987	Ovshinsky et al.		
	A20	6,236,587 B1	05/2001	Gudesen et al.		
	A21	US/2002/0028541 A1	03/2002	Lee et al.		
	A22	6,208,545	03/2001	Leedy		
	A23	6,560,152 B1	05/2003	Cernea		
	A24	5,925,996	07/20/99	Murray		
	A25	6,055,180	04/25/00	Gudesen et al.		
	A26	5,961,215	10/05/99	Lee et al.		
	A27	5,278,796	02/11/94	Tillinghast et al.		
	A28	3,851,316	11/26/74	Kodama		
	A29	4,646,269	02/24/87	Wong et al.		
	A30	4,873,669	10/10/89	Furutani et al.		
	A31	5,383,157	01/17/95	Phelan		
	A32	4,744,061	05/10/88	Takemae et al.		
	A33	6,034,918	03/07/00	Farmwald et al.		
	A34	6,185,712	02/06/01	Kirihata et al.		
	A35	6,070,222	05/30/00	Farmwald et al.		
DL	A36	6,212,121	04/03/01	Ryu et al.		

EXAMINER <i>David J. Lee</i>	DATE CONSIDERED 2/05
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 DEC 01 2003	SERIAL NO. 10/676,862	CASE NO. 10519-112
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(use several sheets if necessary)		APPLICANT(S): So et al.

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER <small>Number-Kind Code (if known)</small>	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
DL	A37	4,698,788	10/06/87	Flannagan et al.		
	A38	5,276,649	01/04/94	Hoshita et al.		
	A39	6,385,074 B1	05/2002	Johnson et al.		
	A40	6,373,768 B2	04/16/2002	Woo et al.		
	A41	5,107,139	04/21/1992	Houston et al.		
	A42	5,359,571	10/1994	Yu		
	A43	5,410,512	04/1995	Takase et al.		
	A44	5,940,340	08/1999	Ware et al.		
	A45	4,592,027	05/1986	Masaki		
	A46	US 2003/0043643 A1	03/2003	Scheuerlein et al.		
	A47	6,507,238	01/2003	Yang		
DL	A48	6,577,549	06/2003	Tran et al.		

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
DL	A49	"A 14ns 1Mb CMOS SRAM with Variable Bit-Organization," Wada et al., 1988 IEEE International Solid-State Circuits Conference, pages 252-253 (February 19, 1988).
	A50	"Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operation," U.S. Patent Application Serial No. 09/748,649, filed December 22, 2000; inventors: Roy E. Scheuerlein and Matthew P. Crowley.
	A51	"64M x 8 Bit NAND Flash Memory," Samsung Electronics (October 27, 2000).
	A52	"How Flash Memory Works," wysiwyg://8/http://www.howstuffworks.com/flash-memory.htm?printable=1, 5 pages (1998).
	A53	"Datalight FlashFX™ 4.06 User's Guide," page 11 (August 2000).
	A54	"How Does TrueFFS® manage Wear Leveling?," http://www.m-sys.com/content/information/calclnfo.asp , 2 pages (printed October 5, 2001)
	A55	"A CMOS Bandgap Reference Circuit with Sub-1V Operation," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999, pages 670-674.
	A56	"Sub-1V CMOS Proportional to Absolute Temperature References," IEEE Journal of Solid-State Circuits, Vol. 38, No.1, January 2003, pages 85-89.
	A57	"The flash memory read path: building blocks and critical aspects," Micheloni et al., Proceedings of the IEEE, Vol. 91, No. 4, April 2003, pages 537-553.
DL	A58	"A current-based reference-generations scheme for 1T-1C ferroelectric random-access memories," Siu et al., IEEE Journal of Solid-State Circuits, Volume 38 Issue 3, March 2003, pages 541-549.

EXAMINER <i>[Signature]</i>	DATE CONSIDERED 2/05
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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE 09/30/2003	GROUP ART UNIT 2186
(use several sheets if necessary)		APPLICANT(S): So et al.

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
DL	A1	6,754,124	6/22/2004	Seyyedy et al.		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	

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